

Docket No.: 50090-295

**PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Masaki WATANABE, et al.

Serial No.: 09/846,272

Filed: May 02, 2001

For: SEMICONDUCTOR DEVICE HAVING CAPACITORS FOR REDUCING POWER SOURCE NOISE



Group Art Unit: 2827

Examiner: L.C. Cruz

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THE COMMISSIONER FOR PATENTS AND TRADEMARKS  
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

- ☒ No additional fee is required.  
☐ Applicant is entitled to small entity status under 37 CFR 1.27  
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	15	20	0	\$18.00 =	\$0.00
Independent Claims	3	3	0	\$84.00 =	\$0.00
Multiple claims newly presented					\$0.00
Fee for extension of time					\$0.00
Total of Above Calculations					\$0.00

- ☐ Please charge my Deposit Account No. 500417 in the amount of \$0.00. An additional copy of this transmittal sheet is submitted herewith.
- ☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

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Date: October 18, 2002

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**PATENT**  
#916  
10/23/2  
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**AMENDMENT**

Commissioner for Patents  
Washington, DC 20231

Sir:

The following amendments and remarks are respectfully submitted in response to  
the Office Action dated July 19, 2002.

**IN THE SPECIFICATION:**

Please replace the paragraph beginning at page 2, line 23, with the following  
rewritten paragraph:

91  
The BGA type semiconductor device is at its limit of fabrication when coming to  
measure about 40 mm per side. When large-sized devices carry numerous terminals, they  
may adopt a pin grid array structure. The pin grid array structure, however, requires  
installing a socket between the semiconductor chip and the mounting substrate, which raises  
fabrication costs.